

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Gattiker DOCKET NO.: AUS920030653US1
SERIAL NO: (Not Yet Assigned) EXAMINER: (Not Yet Assigned)
FILED: (herewith) ART UNIT: (Not Yet Assigned)
TITLE: METHOD AND SYSTEM FOR ANALYZING QUIESCENT POWER PLANE
CURRENT (IDDQ) TEST DATA IN VERY-LARGE SCALE INTEGRATED (VLSI)
CIRCUITS

MAIL STOP PATENT APPLICATION
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Scottsdale, AZ 85251-3989

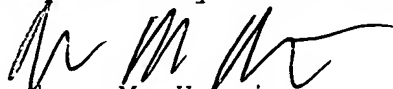
Dear Sir:

INFORMATION DISCLOSURE STATEMENT

This Information Disclosure Statement is submitted in regards to the above-identified patent application. A PTO-SB/08 form is attached along with copies of the references cited therein.

No fee is believed to be required in connection with this Information Disclosure Statement. However, if there are any fees incurred by this transmittal, please deduct them from IBM Deposit Account NO. 09-0447.

Respectfully submitted,



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Sheet	1	of	3
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Complete if Known

Application Number

Filing Date

First Named Inventor

Gattiker

Art Unit

Examiner Name

Attorney Docket Number

AUS920030653US1

U. S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

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		Applicant Number	
		Filing Date	
		First Named Inventor	Gattiker
		Art Unit	
		Examiner Name	
Sheet 2 of 3	Attorney Docket Number	AUS920030653US1	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		KRUSEMAN, ET AL. The Future of IDDQ Testing, IEEE International Test Conference Proceedings, 2001	
		THIBEAULT, Improving Delta-IDDQ-based Test Methods, IEEE International Test Conference Proceedings, 2000	
		MAXWELL,, ET AL. Current Ratios: A Self-Scaling Technique, IEEE International Test Conference Proceedings, 1999	
		GATTIKER,, ET AL. Current Signatures, IEEE VLSI Test Symposium Proceedings, 1996	
		OKUDA, Eigen-Signatures for Regularity-based IDDQ Testing, IEEE VLSI Test Symposium Proceedings, 2002	
		OKUDA, DECOUPLE: Defect Current Detection in Deep Sub-micron IDDQ, IEEE International Test Conference Proceedings, 2000	
		VARIYAM, Increasing the IDDQ Test Resolution Using Current Prediction, IEEE International Test Conference Proceedings, 2000	
		BERGMAN, ET AL., Improved IDDQ Testing With Empirical Linear Prediction, IEEE International Test Conference Proceedings, 2002	
		HENRY, ET AL., Burn-in Elimination of a High Volume Microprocessor Using IDDQ, IEEE International Test Conference Proceedings, 1996	
		NIGH, Application and Analysis of IDDQ Diagnostic Software, IEEE International Test Conference Proceedings, 1997	

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Examiner Name

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3

of

3

Attorney Docket Number

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		LAVO, ET AL., Eliminating the Ouija Board: Automatic Thresholds and Probabilistic IDDQ Diagnosis, IEEE International Test Conference Proceedings, 1999	
		GATTIKER, Current Signatures for Integrated Circuit Test Strategy Advisor, Carnegie Mellon University, Ph.D. Dissertation	

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